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EXAMINER	
THOMPSON, JR, OTIS L	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/520,691	SHI, XINMING	
	Examiner	Art Unit	
	OTIS L. THOMPSON, JR	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed November 4, 2008, with respect to claim 1, have been fully considered but they are not persuasive. Regarding claim 1, Applicant argues that Byers et al. teaches routing at Layer 3 while the claimed invention teaches switching at Layer 2. Applicant cites Byers et al., column 3 lines 15-30 to support this argument. However, the non-final rejection dated August 5, 2008 clearly cites, in section 5, Column 1 lines 40-54, which teaches *a centralized exchanging and controlling unit that utilizes a HUB structure or a switch structure.* Although this teaching exists in Byers et al. as background art to the claimed invention of Byers et al., it still constitutes prior art and can be relied upon as a grounds of rejection. Since Byers et al. teaches *a HUB structure or a SWITCH structure to perform functionalities* (Column 1 lines 40-50, see "...central high-speed fabric or hub to switch traffic between all modules...central fabric, in a star topology..."), the current rejection of claim 1 over Byers et al. is maintained.

2. Applicant's arguments filed November 4, 2008, with respect to claim 6 and 10: *presetting a state of address pins, each of the modules getting its own address by reading the current state of its own address pins*, have been fully considered but they are not persuasive. Applicant argues that Smith (Non-Final rejection dated August 5, 2008, Section 10) fails to teach this limitation because the geographic address information in Smith is dedicated to PCI bus addressing, and the geographic address has to be used in conjunction with other addresses in order to differentiate among the memory windows of various server blades. While this may be true in Smith, Examiner

respectfully asserts that it is irrelevant to the following feature as claimed: *presetting a state of address pins, each of the modules getting its own address by reading the current state of its own address pins.* As correctly stated by Applicant, Smith teaches that geographic address information (of address pins) is read to uniquely identify a system or blade (i.e. a module) (i.e. *presetting a state of address pins, each of the modules getting its own address by reading the current state of its own address pins*, Also see Claim 1 of Smith). Any other teaching in Smith that provides for use of the geographic address information for any other reason than addressing a module is irrelevant because those other teachings do not alter the geographic address information of the module itself. In other words, the geographic address information may be used in combination with other addresses in some way to differentiate among the memory windows, but this use does not change the way the address of a module is known (i.e. obtaining address from state of address pins, i.e. geographic address information). Therefore, the rejection of the aforementioned feature in claim 6 is maintained.

3. Applicant's arguments filed November 4, 2008, with respect to claims 6 and 10: *wherein the destination address is an address of the destination module* ***obtained by reading the current state of the address pins of the destination module***, have been fully considered but they are not persuasive. Applicant argues that Gleeson does not teach this feature. Examiner agrees but also notes that Smith actually teaches *obtaining the address of a module by reading the current state of pins* (Smith, Claim 1).

Applicant further asserts that the combination of Byers et al., Smith, and Gleeson would not arrive at claim 6 or 10. Examiner disagrees. Byers et al. teaches a fabric-based system in a star topology with modules connecting to a backplane, Smith teaches the addressing of modules connected to a backplane, and Gleeson teaches the communication between modules connected to a centralized exchanging and controlling unit. Thus, combination of the three would yield claim 6. Furthermore, while Gleeson is directed toward a network consisting of a switch with connected nodes, it is obvious that the same process can be applied to the fabric-based star topology backplane system with separately connected modules. It is further noted that Applicant relates and compares the instant application to a network switch type application (such as Gleeson et al.) on pages 4-6 where Applicant discusses a HUB or SWITCH structure consisting of Ethernet interfaces.

The detailed action below is updated to reflect the amendments to the claims.

DETAILED ACTION

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, and 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Byers et al. (US 6,693,901 B1).

6. **Regarding claim 1,** Byers et al. teaches the claimed invention in the BACKGROUND OF THE INVENTION section of the patent. Byers et al. teaches a fabric based backplane system which uses a central high-speed fabric or hub to switch (i.e. *centralized exchanging and controlling unit utilizes a HUB structure or a SWITCH structure to perform its functionalities*) traffic between modules (i.e. *sending a message to the centralized exchanging and controlling unit by a source module, processing the message by the centralized exchanging and controlling unit, and forwarding the processed message to a destination module by the centralized exchanging and controlling unit*) (Column 1 lines 42-46). The modules are connected to the central fabric over a cable or backplane in a star topology (i.e. *connecting the centralized exchanging and controlling unit with each of the modules in the device through a communication control interface of the module*) (Column 1 lines 42-46). It is well known in the art that in a star topology, each module has a separate physical interface or connection to the central fabric. Byers et al. does not specifically teach a step of *setting a centralized exchanging and controlling unit in the device,* however, the setting step is inherent in the fabric based backplane system because it allows the modules of the system to communication with each other (Column 1 lines 49-51, see "...full central fabric...must be installed before any modules can be interconnected...").

While fabric based backplane systems are costly, as taught by Byers et al. (Column 1 lines 49-54), the central fabrics of these systems provide large bandwidths needed to support high-speed computer or broadband communications (Column 1 lines 46-49).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to modify the teachings of Byers et al. in order to employ a high-speed large bandwidth system (fabric based backplane) needed to support high-speed computer or broadband communications.

7. **Regarding claim 2,** Byers et al. discloses the claimed invention above but does not specifically disclose *broadcasting the message by the centralized exchanging and controlling unit, comparing, by each of the modules, the destination address of the message with an address of the module, and if the two addresses are identical, receiving the message by the module.*

However, it is well known in the art that when broadcasting a message, whether in a system device or in a network, a module or node, whose address matches the destination address indicated in the broadcast message, receives the message while other modules or nodes discard the message if the addresses do not match. This is advantageous in that the *centralized exchanging and controlling unit* does not have to perform any processing on the message, thereby reducing communication delay in broadcasting. The *centralized exchanging and controlling unit* only has to forward the message to all the modules or nodes, and the modules or nodes perform necessary processing to determine if the message is addressed thereto.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to modify Byers et al. to include broadcasting from the central fabric and destination matching at the separately connected modules in

order to keep the central fabric from having to perform any processing on messages, thereby decreasing communication delay.

8. **Regarding claim 5,** Byers et al. discloses *sending the message from the source module to the destination module directly through exchanging by the centralized exchanging and controlling unit* (Column 1 lines 42-46, see "…central high-speed fabric or hub to switch traffic between all modules...").

9. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byers et al. as applied to claim 2 above, and further in view of Smith (US 6,792,515 B2).

10. **Regarding claims 3 and 4,** Byers et al. discloses the claimed invention above but fails to specifically disclose *presetting address pins of each of the modules in the device, and each of the modules in the device getting address of the module by reading a current state of the address pins of the module* and *presetting the state of address pins in each of the modules by setting a voltage state on a backplane circuit.*

However, Smith discloses a system in which CPU-based systems are connected to a single PCI bus, through a backplane connection (Column 1 lines 55-60; Figure 2). The address of the CPU-based system is defined by the state of a set of geographic address pins of a connector that connects the CPU-system to the peripheral bus (i.e. *presetting address pins of each of the modules by reading the current state of address pins*) (Claim 1, see "...wherein the geographic address..."). Smith further discloses that each of the geographic address pins is physically tied to either a logical low voltage (ground) or a logical high voltage (Vcc) at the connector, and the geographic address is

determined by the binary number defined by the pins (i.e. *presetting the state of address pins in each of the modules by setting a voltage state on a backplane circuit*) (Column 4 lines 55-61). Smith is advantageous in that it allows processors to communicate with one another without having to incorporate any signification memory mapping hardware (Column 6 lines 43-47).

The motivation to combine the teachings of Byers et al. and Smith lies the fact that both inventions are directed toward backplane systems, and a backplane is typically constructed of a multi-layer circuit board with conductive traces selectively routed to provide the high-speed interconnection. Connectors are provided on the backplane to couple circuit boards, packs, or modules which are held in place by a slotted chassis (Byers et al., Column 1 lines 14-17). Hence, it is obvious that the fabric-based star topology backplane system taught by Byers et al. could perform the same steps, in setting the address pins of each module, as those steps of Smith cited in the previous paragraph.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to incorporate the addressing method of Smith into Byers et al. in order to allow modules in a fabric-based backplane system to communicate with one another without having to incorporate significant memory mapping hardware into the system.

11. Claims 6-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byers et al. in view of Smith and further in view of Gleeson et al. (US 6,763,023).

12. **Regarding claims 6 and 10,** Byers et al. teaches *a method and device for realizing communication between modules of a system device, wherein a centralized exchanging and controlling unit is set in the system device and connected with each module of the system device separately through a respective communication control interface of each module* in the BACKGROUND OF THE INVENTION section of the patent. Specifically, Byers et al. teaches a fabric based backplane system which uses a central high-speed fabric or hub to switch traffic between modules (i.e. *centralized exchanging and controlling unit and communication between the modules of the device*) (Column 1 lines 42-46). The modules are connected to the central fabric over a cable or backplane in a star topology (i.e. *connected with each module of the system device separately through a respective communication control interface of each module*) (Column 1 lines 42-46). It is well known in the art that in a star topology, each module has a separate physical interface or connection to the central fabric. Byers et al. does not specifically teach a step of *setting a centralized exchanging and controlling unit in the device,* however, the setting step is inherent in the fabric based backplane system because it allows the modules of the system to communication with each other (Column 1 lines 49-51, see "...full central fabric...must be installed before any modules can be interconnected..."). While fabric based backplane systems are costly, as taught by Byers et al. (Column 1 lines 49-54), the central fabrics of these systems provide large bandwidths needed to support high-speed computer or broadband communications (Column 1 lines 46-49).

Byers et al. does not teach or suggest *presetting address pins of each of the modules in the device, each of the modules in the device getting address of the module by reading a current state of the address pins of the module, and obtaining the address of the destination module by reading the current state of the address pins of the destination module.*

However, Smith discloses a system in which CPU-based systems are connected to a single PCI bus, through a backplane connection (Column 1 lines 55-60; Figure 2). The address of the CPU-based system is defined by the state of a set of geographic address pins of a connector that connects the CPU-system to the peripheral bus (i.e. *presetting address pins of each of the modules by reading the current state of address pins*, i.e. *and obtaining the address of the destination module by reading the current state of the address pins of the destination module*) (Claim 1, see "...wherein the geographic address..."). Smith is advantageous in that it allows processors to communicate with one another without having to incorporate any signification memory mapping hardware (Column 6 lines 43-47).

The motivation to combine the teachings of Byers et al. and Smith lies the fact that both inventions are directed toward backplane systems, and a backplane is typically constructed of a multi-layer circuit board with conductive traces selectively routed to provide the high-speed interconnection. Connectors are provided on the backplane to couple circuit boards, packs, or modules which are held in place by a slotted chassis (Byers et al., Column 1 lines 14-17). Hence, it is obvious that the fabric-based star topology backplane system taught by Byers et al. could perform the same

steps, in setting the address pins of each module, as those steps of Smith cited in the previous paragraph.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to incorporate the addressing method of Smith into Byers et al. in order to allow modules in a fabric-based backplane system to communicate with one another without having to incorporate significant memory mapping hardware into the system.

Byers et al. in view of Smith does not specifically disclose *sending a message carrying a destination address to the centralized exchanging and controlling unit by a source module, processing the message by the centralized exchanging and controlling unit, and forwarding the processed message to a destination module by the centralized exchanging and controlling unit to the destination address, wherein the destination address is an address of the destination module.*

However, Gleeson et al. discloses this process being performed in a network switch illustrated in figure 3. In step 31, a packet containing a destination address is received at a network switch from a source. In step 34, the destination address of the packet is compared against addresses in a database to see if a match is found. If a match is found, then in step 35 the packet is forwarded to the destination using the destination address indicated by the packet. Although Gleeson et al. is directed toward a network consisting of a switch with connected nodes, it is obvious that the same process can be applied to the fabric-based star topology backplane system with separately connected modules. It is further noted that Applicant relates and compares

the instant application to a network switch type application (such as Gleeson et al.) on pages 4-6 where Applicant discusses a HUB or SWITCH structure consisting of Ethernet interfaces. Gleeson et al. is advantageous in that it incorporates the learning of addresses at the network switch (Column 3 lines 66-67), which obviously enables the switch to perform quick switching and processing decisions based on destination addresses indicated in packets.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to incorporate the switching process of Gleeson et al. into the system of Byers et al. in view of Smith in order to allow the fabric of the star topology backplane system to perform quick decisions processing and forwarding messages between modules.

13. **Regarding claims 7 and 11,** Byers et al. in view of Smith and further in view of Gleeson et al. discloses *broadcasting the message by the centralized exchanging and controlling unit to all the modules in the system device* (Gleeson et al., Figure 3 step 36; Column 4 lines 23-40, see "…'flood' or 'broadcast' the packet…to all ports…") *and comparing the destination address carried in the message with its own address by each of the modules in the system device, and if the two addresses are identical, receiving the message by the module* (Gleeson et al., Column 4 lines 23-40, see "...response from a device having the network address identified in the packet...").

14. **Regarding claims 8 and 12,** Byers et al. in view of Smith and further in view of Gleeson et al. discloses *presetting the state of address pins in each module by setting a voltage station on a backplane circuit.* Specifically, Smith discloses an addressing

method in which each of the geographic address pins (See section 9 above) is physically tied to either a logical low voltage (ground) or a logical high voltage (Vcc) at the connector, and the geographic address is determined by the binary number defined by the pins (i.e. *presetting the state of address pins in each of the modules by setting a voltage state on a backplane circuit*) (Column 4 lines 55-61).

15. **Regarding claims 9 and 13,** Byers et al. in view of Smith and further in view of Gleeson et al. discloses *sending the message from the source module to the destination module directly through the centralized exchanging and controlling unit* (Byers et al., Column 1 lines 42-46, see "…central high-speed fabric or hub to switch traffic between all modules...").

Allowable Subject Matter

16. Claims 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to OTIS L. THOMPSON, JR whose telephone number is (571)270-1953. The examiner can normally be reached on Monday to Thursday 7:30 am to 5:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chirag Shah can be reached on (571)272-3144. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Otis L Thompson, Jr./

Examiner, Art Unit 2419

January 27, 2009

/Chirag G Shah/

Supervisory Patent Examiner, Art Unit 2419